IN THE CLAIMS

All pending claims are herewith presented for the convenience of the Examiner.

Claims 1 – 5 (Cancelled).

6. (ORIGINAL) A method for testing integrated circuits comprising:

providing an excitation voltage to a device;

providing a power supply voltage to the device;

measuring the quiescent power supply current of the device;

changing the power supply voltage to the device; and

determining whether a change in quiescent power supply current of the device exceeds a predetermined allowable change.

7. (ORIGINAL) The method of claim 6 wherein the device is a field effect transistor.

8. (ORIGINAL) The method of claim 6 wherein changing the power supply voltage to the device comprises changing the power supply voltage to one or more predetermined voltages.

9. (ORIGINAL) The method of claim 6 wherein determining whether the change in quiescent power supply current of the device exceeds the predetermined allowable change comprises determining whether (|IDDQ(VCCmax) – IDDQ(VCCmin)|/(Min (IDDQ(VCCmax), IDDQ(VCCmin))) is less than a predetermined value.

10. (ORIGINAL) The method of claim 6 wherein measuring the quiescent power supply current of the device comprises:

determining whether the quiescent power supply current exceeds a maximum predetermined value; and

stopping subsequent testing if the quiescent power supply current exceeds the maximum predetermined value.

11. (ORIGINAL) The method of claim 6 further comprising generating notification data if the change in quiescent power supply current of the device exceeds the predetermined allowable change.

12. (ORIGINAL) A method for testing integrated circuits comprising:

providing an excitation voltage to a device;

providing a power supply voltage to the device;

measuring the quiescent power supply current of the device; and

changing the power supply voltage to the device if the quiescent power supply current is less than a predetermined value.

13. (ORIGINAL) The method of claim 12 further comprising stopping testing if the quiescent power supply current exceeds the predetermined value.

14. (ORIGINAL) The method of claim 12 wherein measuring the quiescent power supply current of the device further comprises waiting a predetermined period of time before measuring the quiescent power supply current of the device.

15. (ORIGINAL) The method of claim 12 wherein the device is a field effect transistor.

16. (NEW) A system for testing semiconductor circuits comprising:

a voltage vector system applying a minimum voltage and a maximum voltage to a drain and a source of a semiconductor device;

a current measuring system measuring a quiescent current of the semiconductor device; and

an IDDQ variation monitor receiving the quiescent current measurement and determining whether a difference in the quiescent current measured at the minimum voltage and the maximum voltage exceeds a predetermined allowable difference.

17. (NEW) The system of claim 16 wherein the minimum voltage comprises VCCmin, the maximum voltage comprises VCCmax, and the IDDQ variation monitor determines whether (|IDDQ(VCCmax) – IDDQ(VCCmin)|/(Min (IDDQ(VCCmax), IDDQ(VCCmin))) is less than the predetermined allowable difference.

18. (NEW) The system of claim 16 further comprising a go/no-go system that performs a go/no-go test prior to the determination performed by the IDDQ variation monitor.

19. (NEW) The system of claim 16 further comprising a go/no-go system that determines whether the quiescent current exceeds a maximum quiescent current.

20. (NEW) The system of claim 16 further comprising:

a go/no-go system that determines whether the quiescent current exceeds a maximum allowable quiescent current; and

wherein the IDDQ variation monitor performs the determination if the quiescent current exceeds the maximum quiescent current.

21. (NEW) The system of claim 16 further comprising:

a go/no-go system that determines whether the quiescent current exceeds a first quiescent current level or a second quiescent current level; and

wherein the IDDQ variation monitor performs the determination if the quiescent current exceeds the first quiescent current, and test failure data is generated if the quiescent current exceeds the second quiescent current level.

22. (NEW) A method for testing semiconductor circuits comprising:

applying a minimum voltage and a maximum voltage to a drain and a source of a semiconductor device with a voltage vector system;

measuring a quiescent current of the semiconductor circuit with a current measuring system at the minimum voltage and the maximum voltage; and receiving the quiescent current measurements at an IDDQ variation monitor and determining whether a difference in the quiescent current measured at the minimum voltage and the maximum voltage exceeds a predetermined allowable difference.

23. (NEW) The method of claim 22 wherein applying the minimum voltage comprises applying VCCmin, applying the maximum voltage comprises applying VCCmax, and the IDDQ variation monitor determines whether (|IDDQ(VCCmax) – IDDQ(VCCmin)|/(Min (IDDQ(VCCmax), IDDQ(VCCmin))) is less than the predetermined allowable difference.

24. (NEW) The method of claim 22 further comprising performing a go/no-go test prior to applying the minimum voltage and the maximum voltage.

25. (NEW) The method of claim 22 further comprising:

applying a test voltage prior to applying the minimum voltage and the maximum voltage; and

terminating the testing of the semiconductor device if the quiescent current while the test voltage is applied is greater than a predetermined maximum current.

26. (NEW) The method of claim 22 further comprising:

applying a test voltage prior to applying the minimum voltage and the maximum voltage; and

terminating the testing of the semiconductor device if the quiescent current while the test voltage is applied is less than a predetermined minimum current.

27. (NEW) The method of claim 22 further comprising:

applying a test voltage prior to applying the minimum voltage and the maximum voltage; and

terminating the testing of the semiconductor device if the quiescent current while the test voltage is applied is less than a predetermined maximum current or greater than a predetermined maximum current.

28. (NEW) The method of claim 22 further comprising:

applying a test voltage prior to applying the minimum voltage and the maximum voltage;

terminating the testing of the semiconductor device if the quiescent current while the test voltage is applied is less than a predetermined maximum current or greater than a predetermined maximum current;

applying the minimum voltage and the maximum voltage if the testing is not terminated.